

APPROVED	O.G. FIG. 6c	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	745

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FIGURE 1

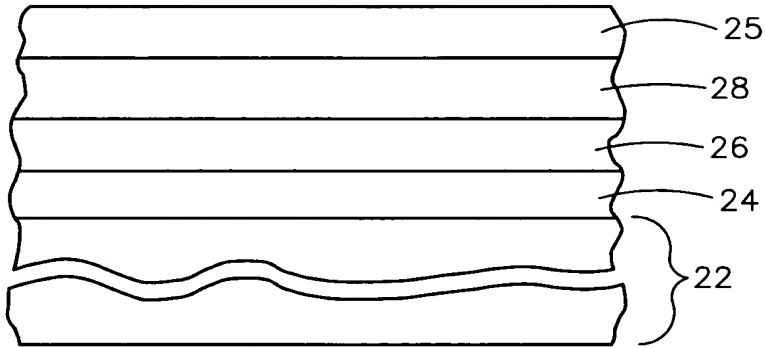
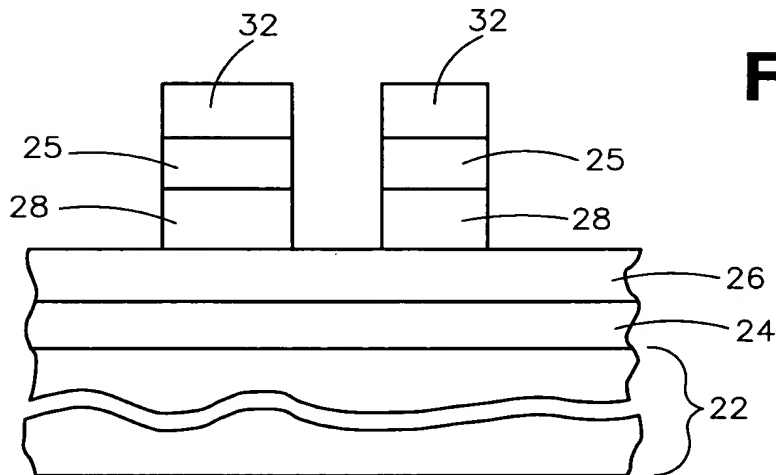


FIGURE 2



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FIGURE 3

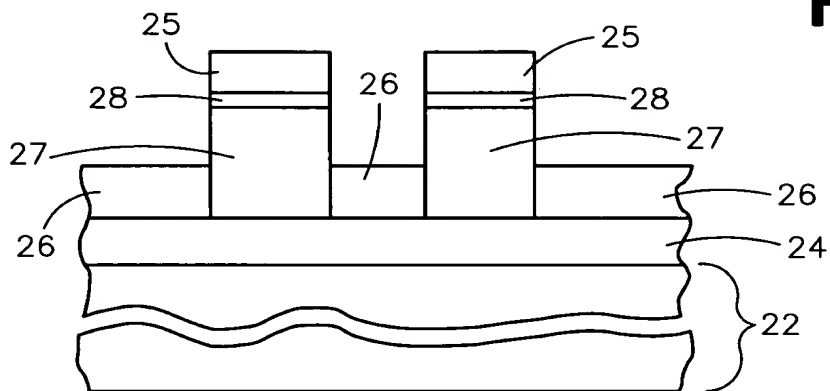
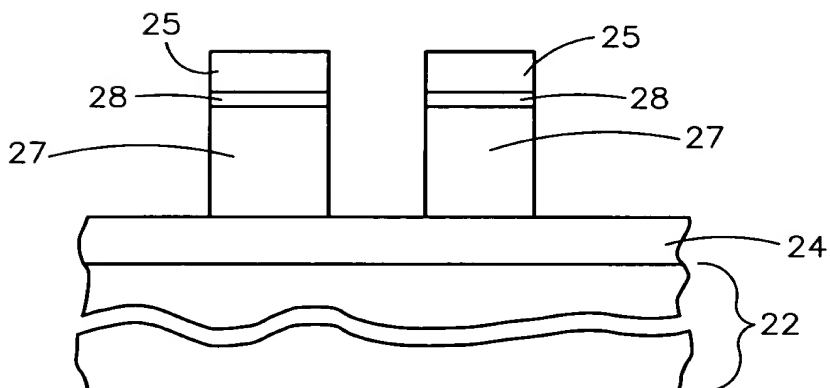


FIGURE 4

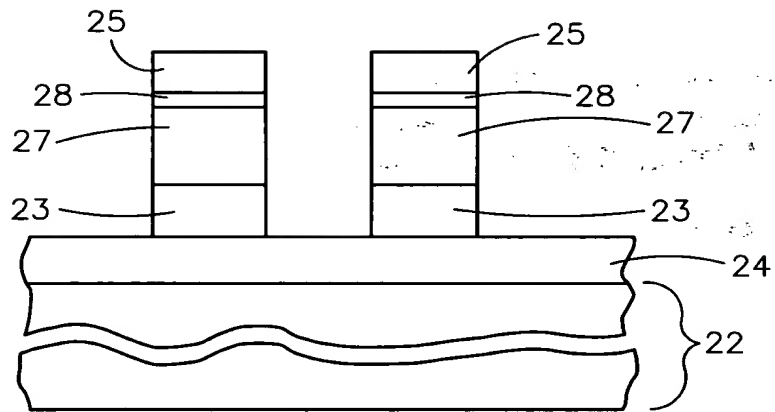


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FIGURE 5



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FIGURE 6A

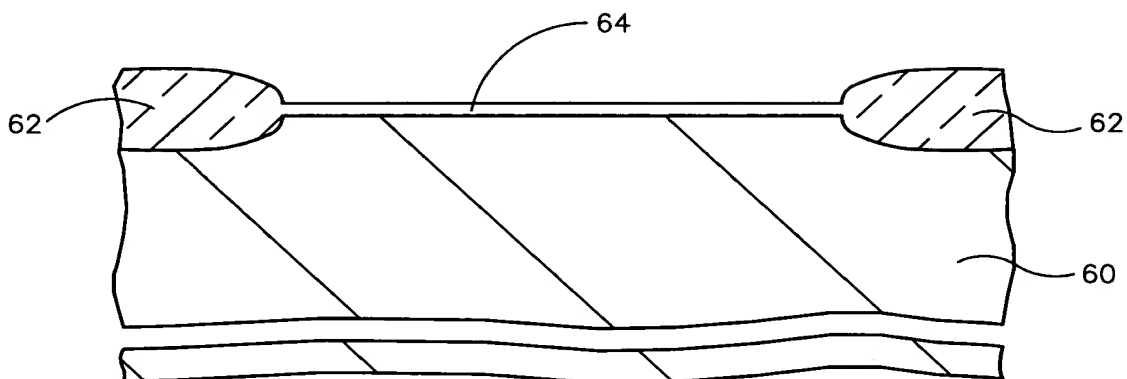
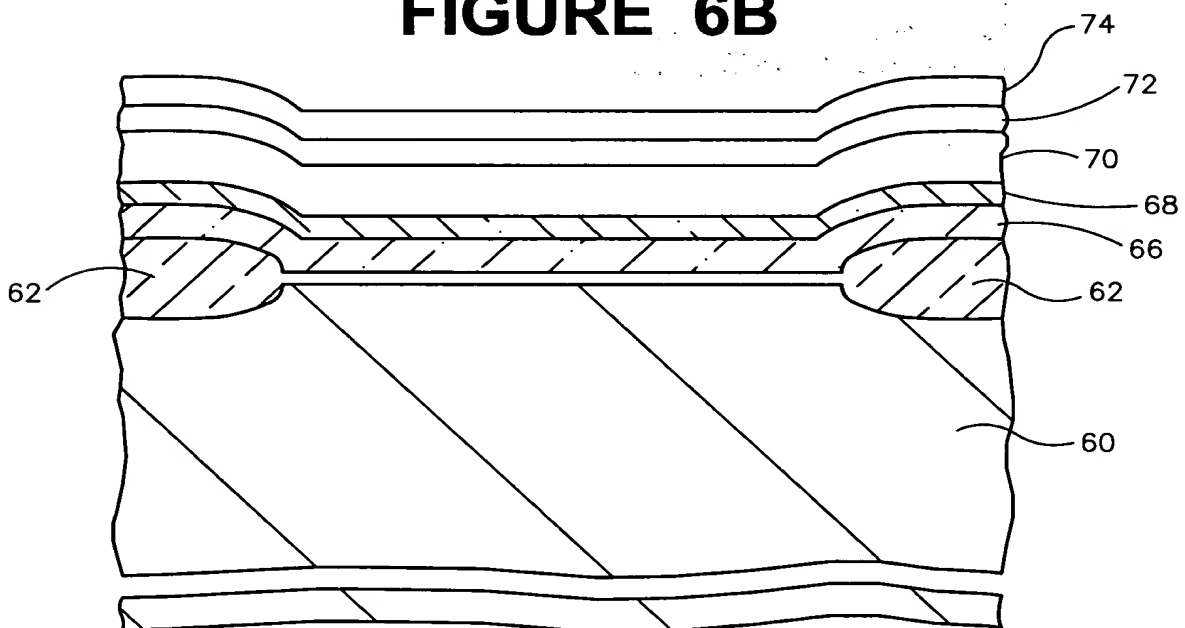


FIGURE 6B

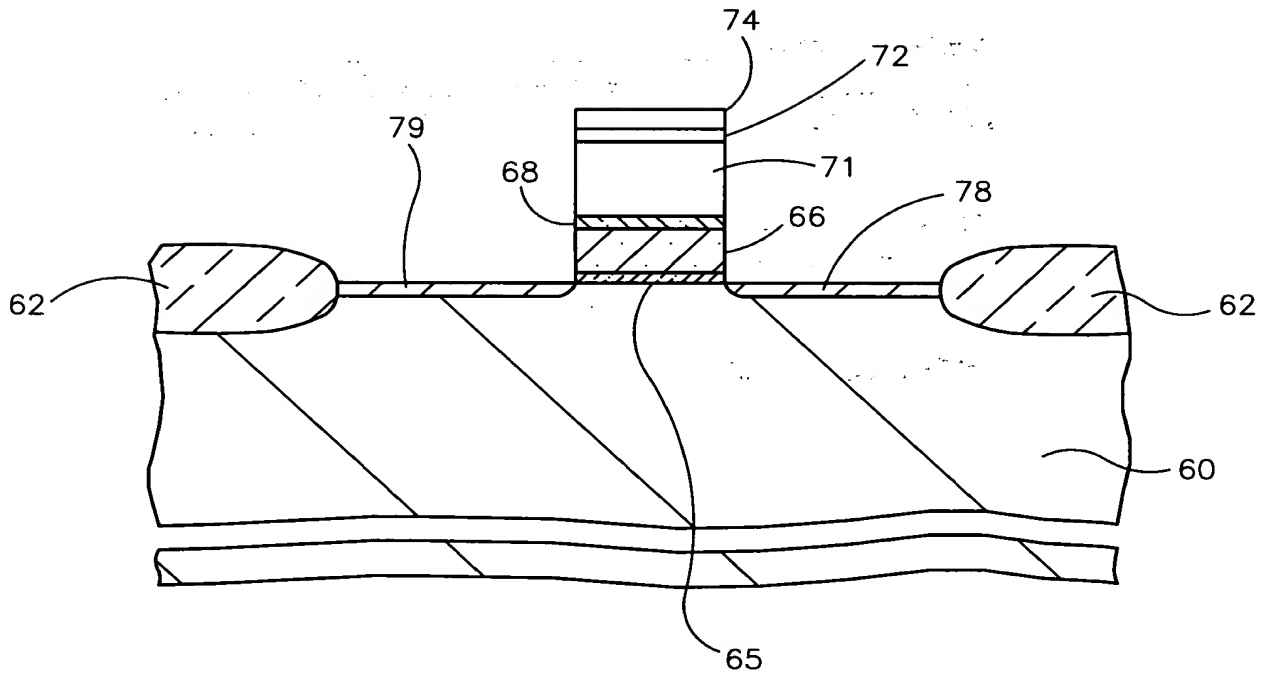


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FIGURE 6C



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FIGURE 7A

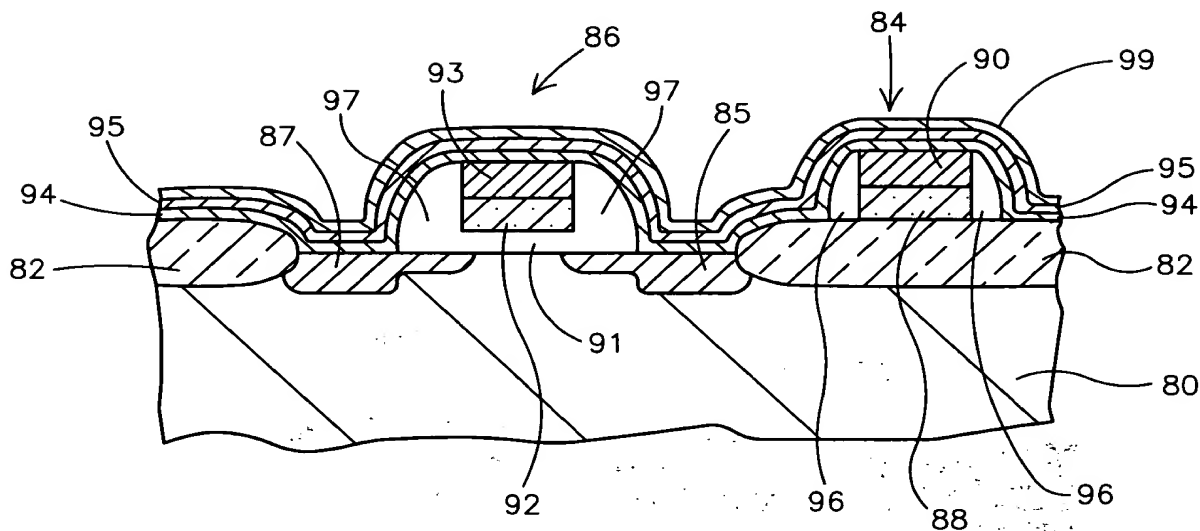
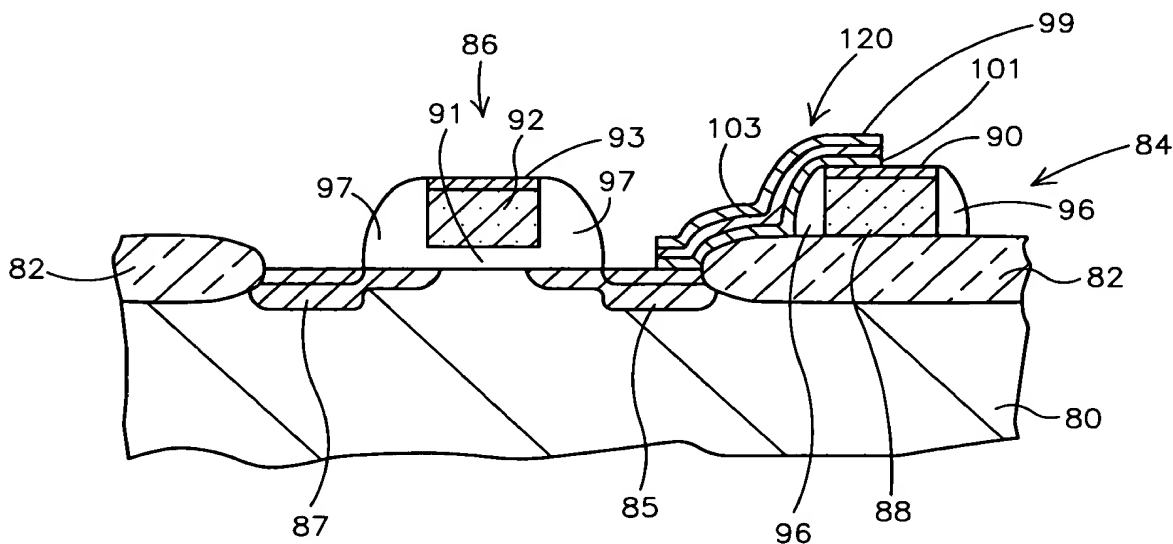


FIGURE 7B



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FIGURE 1

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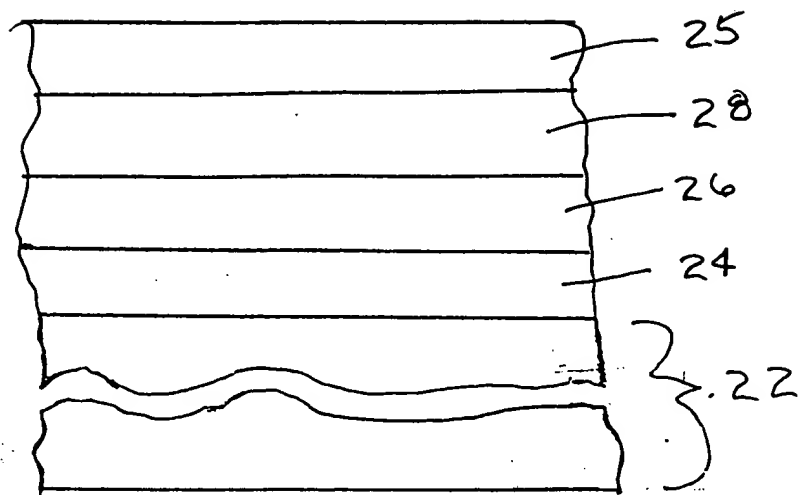


FIGURE 2

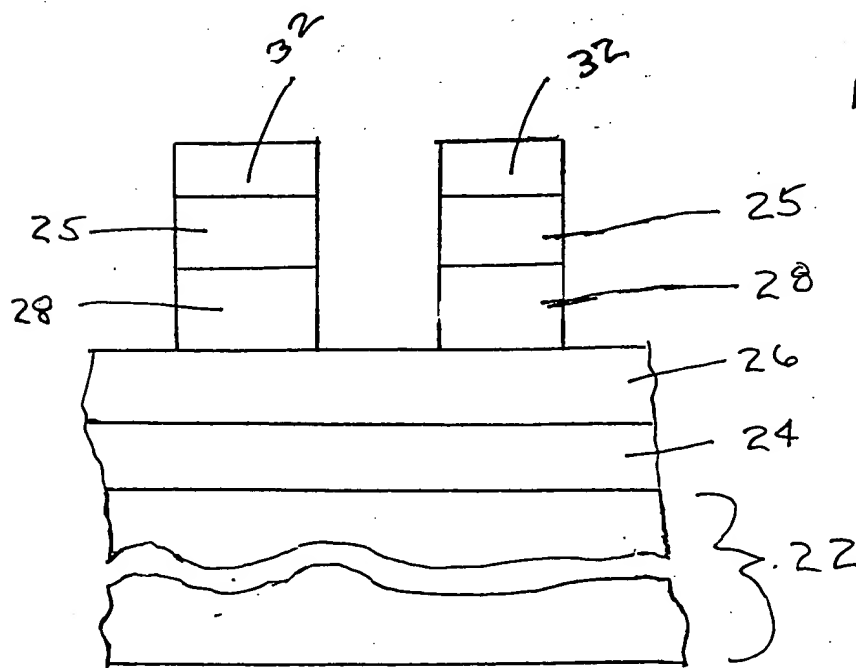


FIGURE 3

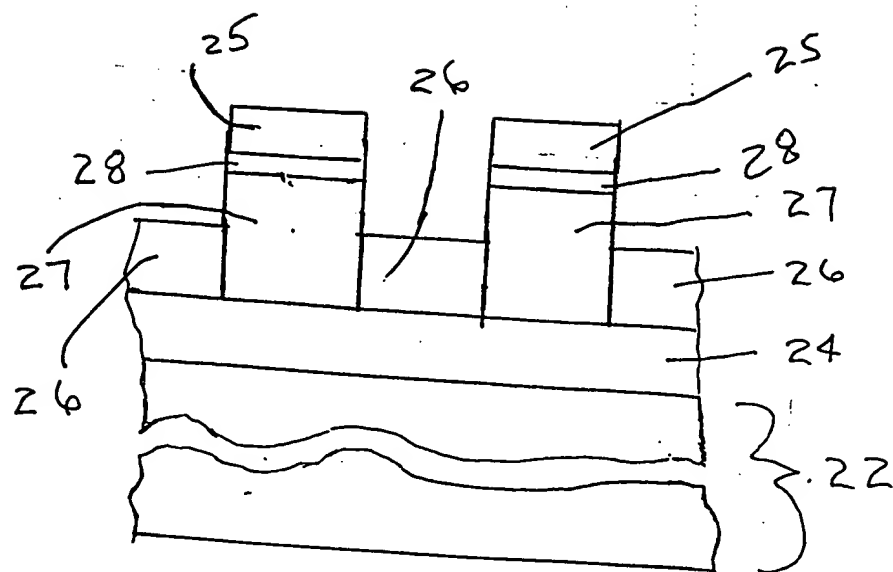


FIGURE 4

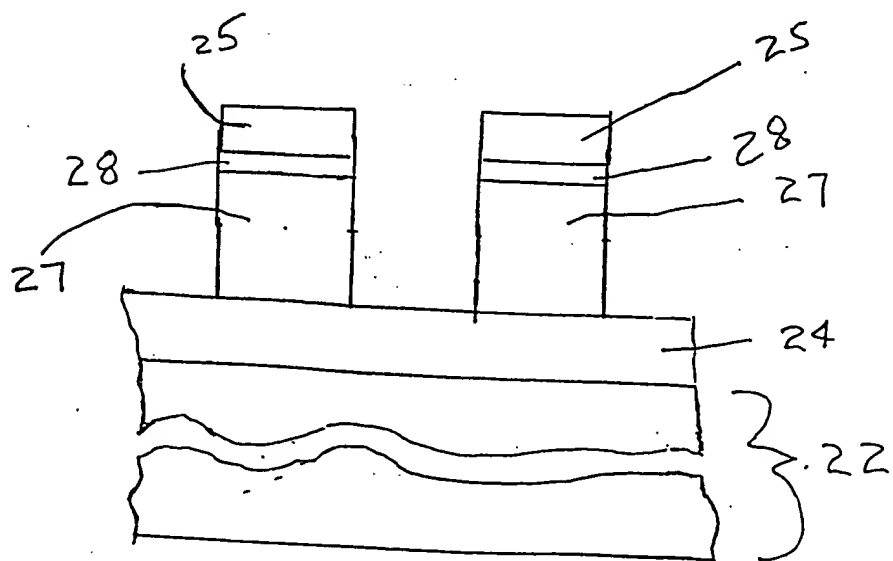


FIGURE 5

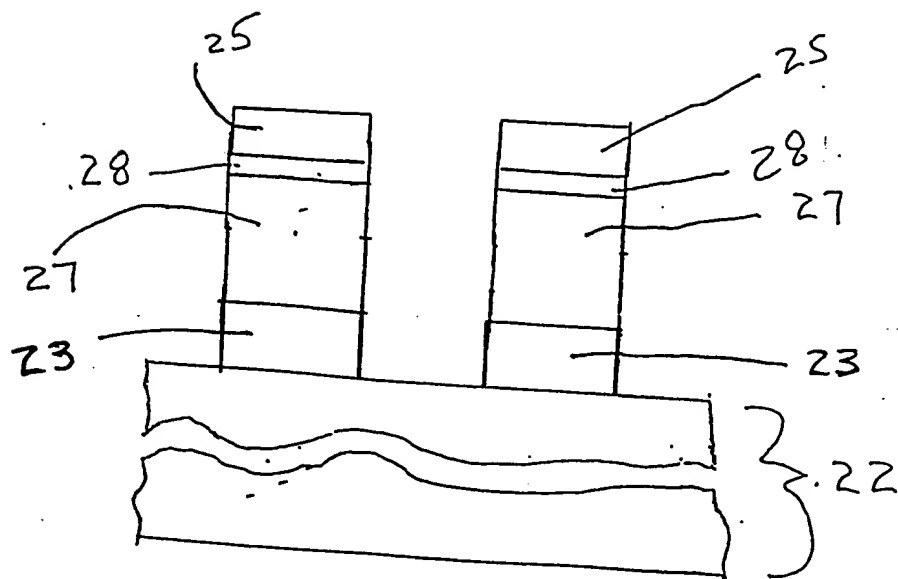


FIGURE 6A

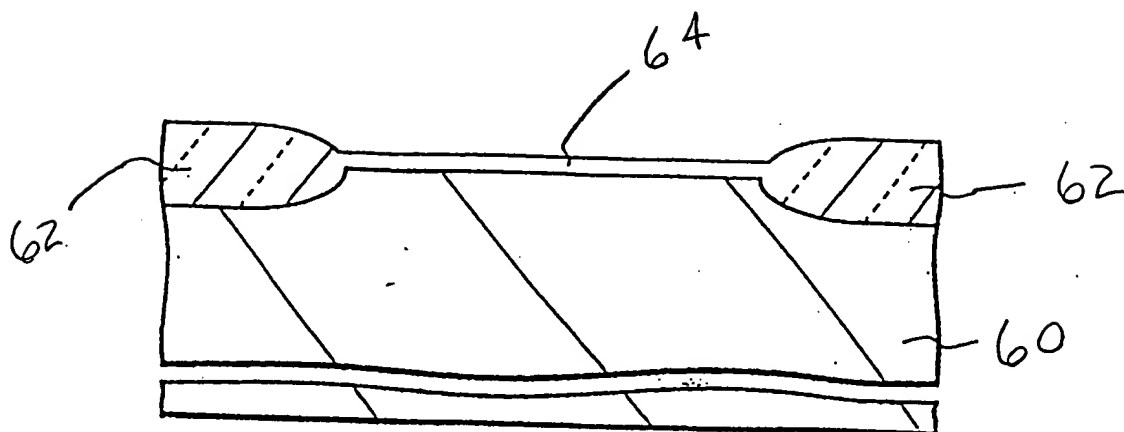


FIGURE 6B

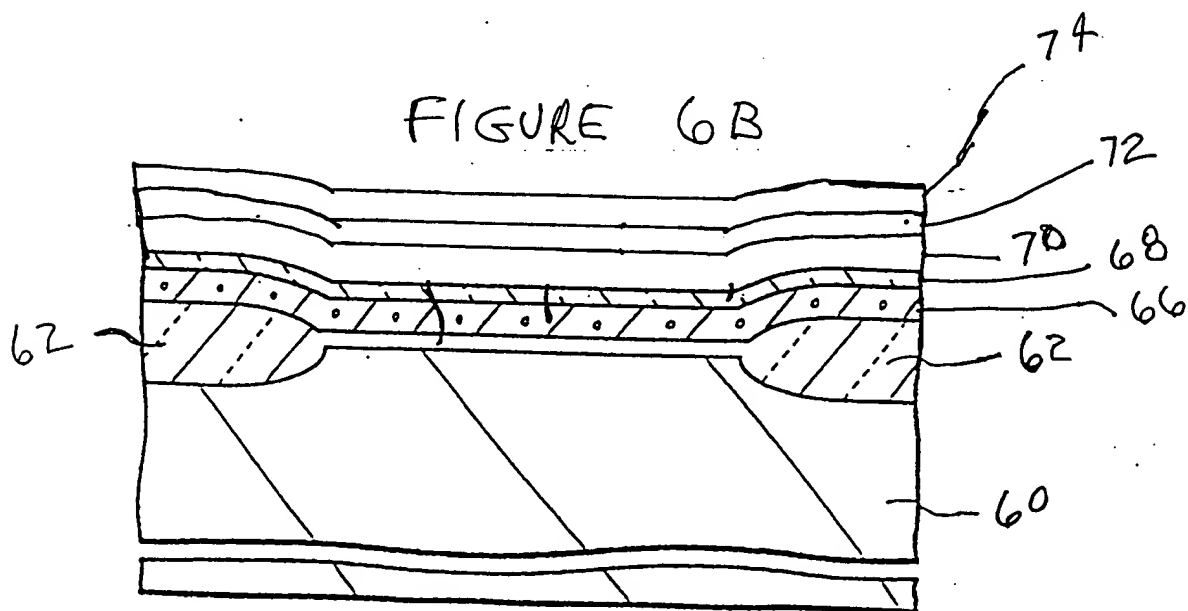
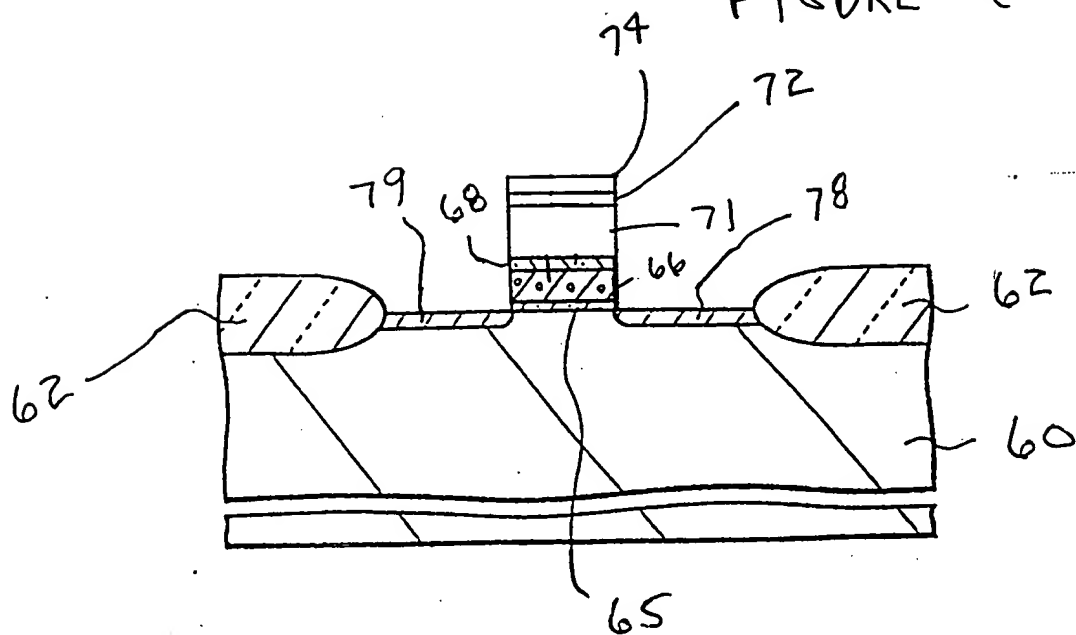


FIGURE 6C



This diagram shows a cross-sectional view of a multi-layered electronic device. It features a central substrate (80) with two main components (91 and 92) mounted on it. Each component is housed within a protective structure (82, 84) and is connected to a network of conductive layers (85, 86, 87, 88, 89, 90, 93, 94, 95, 96, 97, 98, 99). The components are separated by a central gap (90). The entire assembly is supported by a base layer (80).